UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/020,380	10/30/2001	Hassan Hashemi	01CON288PC	4071

25700 7590 01/20/2004

FARJAMI & FARJAMI LLP
16148 SAND CANYON
IRVINE, CA 92618

EXAMINER	
TRAN, THANH Y	
ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 01/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/020,380	HASHEMI ET AL.	
	Examiner	Art Unit	
	Thanh Y. Tran	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for R ply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *91-119* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *111-119* is/are allowed.

6)☒ Claim(s) *91-110* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 91-110 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Applicant's specification fails to teach "a second discrete component embedded in said single interconnect substrate" (emphasis added). This wording is found in independent claim 91. At look at figure 1 yields only an understanding that first and second discrete components 106 surface mounted on the single interconnect substrate 102. None of the drawings of the invention show that a second discrete component embedded in said single interconnect substrate.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 91, 95-96, 98-105, and 107-110 are rejected under 35 U.S.C. 102(b) as being anticipated by Bert et al (U.S. 4,792,773).

With respect to claims 91 and 96, Bert et al teaches an integrated module (Fig. 5) comprising: a single interconnect substrate (comprising elements 1, 9 and 10); a first active circuit chip (2) wire bonded to the single interconnect substrate; a second active circuit chip (3) interconnected to the single interconnect substrate; a first ground plane (a first ground plane is the first part of ground plane 9 connected to metallization 4 as shown in figure 2) integral to the interconnect substrate and operatively associated with the first active chip (2); a second ground plane (a second ground plane is the second part of ground plane 9 connected to metallization 5 as shown in figure 2) integral to interconnect substrate and operatively associated with the second active chip (3); a first discrete component (C') surface mounted on the single interconnect substrate; and second discrete component (C) embedded in the single interconnect substrate.

With respect to claims 95 and 107-108, Bert et al teaches an integrated module (Figs. 2 and 5) wherein at least one (4) of plurality of metal layers (4, 9) defines the first discrete component (2); and wherein the first discrete component (2) is selected from the group consisting of a capacitor (C').

With respect to claims 98-99 and 109-110, Bert et al teaches an integrated module (Fig. 5) wherein at least one (4) of the plurality of metal layers (4, 9) defines a printed component/discrete component (2); and the printed component (2) is selected from the group consisting of a capacitor.

With respect to claim 100, Bert et al teaches an integrated module (Fig. 5) wherein at least one (9) of the plurality of metal layers (4, 9) defines a ground plane (see Fig. 5, element 9, col. 6, lines 34-35).

With respect to claims 101, 102, 104 and 105, Bert et al teaches the first ***active*** circuit chip (2, Figs. 1, 2 and 5) inherently comprises RF & IF sections; and second ***active*** circuit chip (3, Figs. 1, 2 and 5) inherently comprises RF & IF sections. It should be noted that: since chips 2 and 3 are active circuit chips (active components) (see col. 2, lines 45-55 in Bert's reference), they inherently perform the same functions (RF and IF) with the first and second ***active*** circuit chip of the invention.

With respect to claim 103, Bert et al teaches an integrated module (Figs. 2 and 5) further comprising at least one exposed conductive strip (8, Fig. 2) formed on the single interconnect substrate and situated between the first and second active circuit chips (2 and 3), the at least one exposed conductive strip (8, Fig. 2) electrically coupled to at least one (9) of the first and second ground planes. It should be noted that: the at least one exposed conductive strip (8, Fig. 2) electrically coupled to the ground plane 9 by a capacitor C2.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 92-94 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bert et al (U.S. 4,792,773) in view of Hirakawa et al (U.S. 5,652,466).

With respect to claim 92, Bert et al teaches an integrated module (Fig. 5) wherein the first discrete component (C') is surface mounted. Bert et al does not teach the first discrete component (C') is surface mounted ***using a high-temperature solder***. Hirakawa et al teaches an

integrated module (Fig. 1) wherein the first discrete component (8) is surface mounted using a high-temperature solder (see Fig. 1, element 9; col. 4, lines 62-63). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the module of Bert by using a high-temperature solder for attaching the discrete component on the surface of printed circuit board as taught by Hirakawa for preventing short-circuit, which may be caused by melted solder (low-temperature solder), due to the ends of the discrete component.

With respect to claims 93-94, Bert et al does not teach an integrated module further comprising a solder mask area on the single interconnect substrate; the solder mask area is adjacent to the first discrete component.

Hirakawa teaches an integrated module (Fig. 1) further comprising a solder mask area (see the solder area underneath lid 2) on the single interconnect substrate (1); the solder mask area is adjacent to the first discrete component (8). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the module of Bert by including a solder mask area adjacent to the discrete component as taught by Hirakawa for the purpose of securing/retaining the lid to the substrate for protecting the circuit chip.

7. Claim 97 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bert et al (U.S. 4,792,773) in view of Fukuoka (U.S. 5,818,699).

With respect to claim 97, figures 2 and 5 of Bert et al shows that the single interconnect substrate comprises a plurality of metal layers (4, 5, 6, 9 and 10) and a dielectric layer (1).

Bert et al does not teach the single interconnect substrate comprising a plurality of dielectric layers. Fukuoka teaches an integrated module (Fig. 1) comprising a single interconnect substrate (101) wherein the single interconnect substrate (101) comprising a plurality of dielectric layers. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the module of Bert by using a substrate having a plurality of dielectric layers as taught by Hirakawa for the purpose of use in a high density package/module.

8. Claim 106 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bert et al (U.S. 4,792,773).

With respect to claim 106, Bert et al does not teach first active circuit chip comprises a CMOS chip and wherein the second active circuit chip comprises a GaAs chip. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the module of Bert et al by replacing a first active circuit chip with a CMOS chip; and a second active circuit chip with a GaAs chip for the purpose of intended use, since it has been held that a recitation with respect to the manner in which a clamed apparatus is intended to be employed does not differentitate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987).

Allowable Subject Matter

9. Claims 111-119 are allowed.

The following is an examiner's statement of reasons for allowance:

Claims 2, 6 and 26 recite, inter alia,

Claims 111-119 recite, inter alia, "the conductive strip situated between the first and second active circuit chips; a metal lid covering the first and second active circuit chips, the metal lid contacting the conductive ring and the conductive strip, wherein the metal lid, the conductive ring, and the conductive strip substantially prevent electromagnetic interference from reaching the first and second active circuit chips".

The structural combination of the teaching of references: Fukuoka (U.S.5,818,699), Sunahara (U.S.6,153,290), Bert et al (U.S. 4,792,773) and Hirakawa et al (U.S. 5,652,466) do not teach the above limitations.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

Applicant's arguments with respect to claims 91-110 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (703) 305-4757. The examiner can normally be reached on Monday through Thursday and on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo, can be reached on (703) 308-1233. The fax phone number for the organization where this application or proceeding is assigned is (703) 305-3431.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

KAMAND CUNEO

TYT